In the Specification

Please replace paragraph [0001] with the following:

[0001] This application is a continuation of U.S. Patent Application No. 09/634,927, filed August 8, 2000, now U.S. Patent Number 6,360, 356, which is a continuation of U. S. Patent Application No. 09/015,602, filed January 30, 1998, now U.S. Patent Number 6,145,117.

In the Claims

Claims 1 and 2 stand as originally submitted. Please add claims 3-37.

1. A method for transforming a logical hierarchy associated with a model of an electronic design into a physical hierarchy optimized for chip-level implementation of that electronic design, the method comprising:

partitioning the model into a number of data-flow-logic partitions and control logic partitions, each partition having a boundary; and

selectively readjusting partition boundaries in response to placement based information thereby forming a physical hierarchy based on connectivity between partitions.

2. A method for partitioning an electronic design into a number of data-flow-logic partitions, the method comprising:

traversing the electronic design to group data operators inter-connected by buses into data-flow-logic partitions, wherein data operators inter-connected by an independent bus system form an independent data-flow partition; and

selectively breaking or merging each of the data-flow-logic partitions based on placement-based information.

3. (New) A method for predicting the physical characteristics of an electronic design before gate-level implementation, the method comprising:

optimizing a network of logic building blocks logically and physically using placement based information to create an accurate model of the electronic design; and